What is claimed is:

1. A multi-port semiconductor memory comprising;

a memory cell array including a plurality of memory cells,

a first bit line pair performing write-in or read-out of complementary data for the memory cells in the memory cell array,

a second bit line pair performing write-in or read-out of complementary data for the memory cells in the memory cell array,

a plurality of first word lines provided for each of the memory cells for selecting the memory cell that is accessed to the first bit line pair from the memory cell array,

a plurality of second word lines provided for each of the memory cells for selecting the memory cell that is accessed to the second bit line pair from the memory cell array,

and a first pull-up circuit that, when data is written in the memory cell that is selected from the first bit line pair, pulls up a low-level side of the concerned first bit line pair.

2. The multi-port semiconductor memory according to claim 1 further comprising a first regulator circuit that regulates lower power potential of the memory cell such that the low-level for the first bit line pair after pull-up is written in the memory cell as low-level.

3. The multi-port semiconductor memory according to claim 1 or 2 further comprising a second pull-up circuit that, when data is written in the memory cell that is selected from the second bit line pair, pulls up a low level side of the concerned

second bit line pair.

4. The multi-port semiconductor memory according to the claim 3 further comprising a second regulator circuit that regulates lower power potential of the memory cell such that the low-level for the second bit line pair after pull-up is written in the memory cell as low level.